09-06-05   /FW/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	10/771630	Docket Number	CNTR.2095
Filed	02/04/04	Group Art Unit	2183
Examiner		Customer No.	23669
Application Title	PIPELINED MICROPROCESSOR, APPARATUS, AND METHOD FOR GENERATING EARLY INSTRUCTION RESULTS		
First Named Inventor	GERARD M. COL		

REQUEST FOR CORRECTED FILING RECEIPT

Mail Stop **Missing Parts**
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Filing Receipt dated 05/05/04 incorrectly omits the priority claim made to a provisional application in the non-provisional application. Please provide a corrected filing receipt that shows the correct Domestic Priority data as claimed by applicant as follows:

This application claims the benefit of serial number 60/445070 filed on 02/04/03.

Attached are:

1) a copy of the first page of the non-provisional application showing the priority claim; and

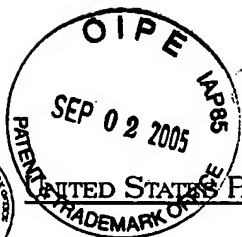2) a copy of the Filing Receipt with corrective markings thereon.

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I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to Mail Stop **Missing Parts**, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,

By: /E. Alan Davis/

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Date:<u>9/2/2005</u>

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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/771,630	02/04/2004	2183	978	CNTR.2095	8	32	5

CONFIRMATION NO. 4117

23669
HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

FILING RECEIPT

OC000000012530109

Date Mailed: 05/05/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Gerard M. Col, Austin, TX;

Assignment For Published Patent Application

VIA Technologies, Inc., Taipei, TAIWAN;

Domestic Priority data as claimed by applicant

Please add:
this application claims the
→ benefit of serial number 60/445070
filed on 02/04/03.

Foreign Applications

If Required, Foreign Filing License Granted: 05/04/2004

Projected Publication Date: 08/04/2005

Non-Publication Request: No

Early Publication Request: No

Title

Pipelined microprocessor, apparatus, and method for generating early instruction results

Preliminary Class

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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PIPELINED MICROPROCESSOR, APPARATUS, AND METHOD

FOR GENERATING EARLY INSTRUCTION RESULTS

by

Gerard M. Col

PRIORITY INFORMATION

[0001]   This application claims priority based on U.S. Provisional Application, Serial No. 60/445070 filed February 4, 2003, entitled EARLY ACCUMULATION OF RESULTS.

FIELD OF THE INVENTION

[0002]   This invention relates in general to the field of pipelined microprocessors, and particularly to early instruction execution therein.

BACKGROUND OF THE INVENTION

[0003]   Modern microprocessors are pipelined microprocessors. That is, they operate on several instructions at the same time, within different blocks or pipeline stages of the microprocessor. Hennessy and Patterson define pipelining as, "an implementation technique whereby multiple instructions are overlapped in execution." Computer Architecture: A Quantitative Approach, 2nd edition, by John L. Hennessy and David A. Patterson, Morgan Kaufmann Publishers, San Francisco, CA, 1996. They go on to provide the following excellent illustration of pipelining:

> A pipeline is like an assembly line. In an automobile assembly line, there are many steps, each contributing something to the construction of the car. Each step operates in parallel with the other steps, though on a